

PSMN2R0-60ES

N-channel 60 V 2.2 m Ω standard level MOSFET in I2PAK

Rev. 02 — 19 April 2011

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in a I2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|--------------------------------|--|--|---------------------|-----|-----|------------|------------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | - | 60 | V | |
| I_D | drain current | $T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1 | [1] | - | 120 | A | |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C};$ see Figure 2 | - | - | 338 | W | |
| T_j | junction temperature | | -55 | - | 175 | °C | |
| Static characteristics | | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see Figure 12 | [2] | - | 1.8 | 2.2 | m Ω |
| | | $V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 100\text{ °C};$ see Figure 12 ; see Figure 13 | - | 3 | 3.5 | m Ω | |
| Dynamic characteristics | | | | | | | |
| Q_{GD} | gate-drain charge | $V_{GS} = 10\text{ V}; I_D = 75\text{ A};$ $V_{DS} = 30\text{ V};$ see Figure 14 ; | - | 32 | - | nC | |
| $Q_{G(tot)}$ | total gate charge | see Figure 15 | - | 137 | - | nC | |
| Avalanche ruggedness | | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ $I_D = 120\text{ A}; V_{sup} \leq 60\text{ V};$ $R_{GS} = 50\text{ }\Omega;$ Unclamped | - | - | 913 | mJ | |

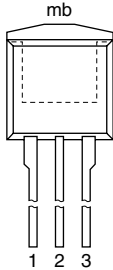
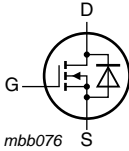


[1] Continuous current limited by package.

[2] Measured 3 mm from package.

2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|---|---|
| 1 | G | gate |  |  |
| 2 | D | drain | | |
| 3 | S | source | | |
| mb | D | mounting base; connected to drain | | |

SOT226 (I2PAK)

3. Ordering information

Table 3. Ordering information

| Type number | Package | | Version |
|--------------|---------|--|---------|
| | Name | Description | |
| PSMN2R0-60ES | I2PAK | plastic single-ended package (I2PAK); TO-262 | SOT226 |

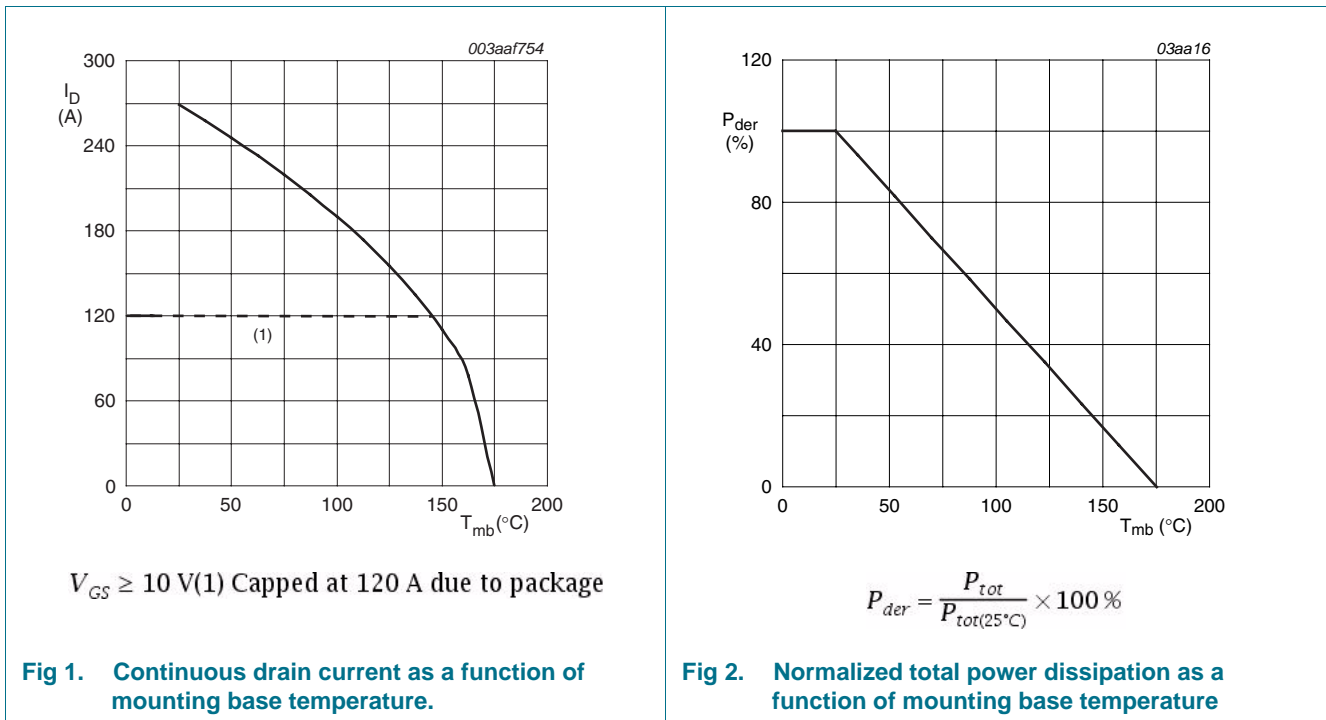
4. Limiting values

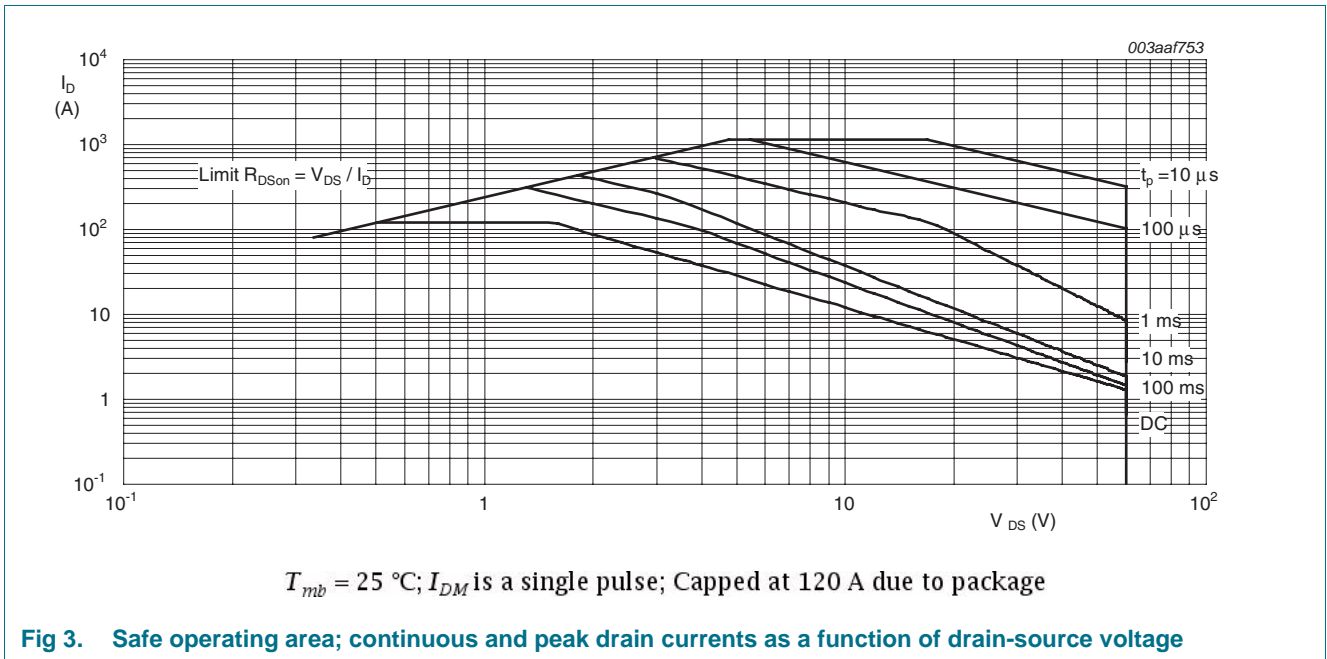
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------|--|--|-----|------|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | 60 | V |
| V_{DGR} | drain-gate voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$ | - | 60 | V |
| V_{GS} | gate-source voltage | | -20 | 20 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C};$ see Figure 1 | [1] | 120 | A |
| | | $V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ see Figure 1 | [1] | 120 | A |
| I_{DM} | peak drain current | pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C};$ see Figure 3 | - | 1135 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C};$ see Figure 2 | - | 338 | W |
| T_{stg} | storage temperature | | -55 | 175 | °C |
| T_j | junction temperature | | -55 | 175 | °C |
| $T_{slid(M)}$ | peak soldering temperature | | - | 260 | °C |
| Source-drain diode | | | | | |
| I_S | source current | $T_{mb} = 25\text{ °C}$ | [1] | 120 | A |
| I_{SM} | peak source current | pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$ | - | 1135 | A |
| Avalanche ruggedness | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 120\text{ A};$ $V_{sup} \leq 60\text{ V}; R_{GS} = 50\text{ }\Omega;$ Unclamped | - | 913 | mJ |

[1] Continuous current limited by package





5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|------------------------------|-----|------|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | 0.22 | 0.44 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Vertical in free air | - | 60 | - | K/W |

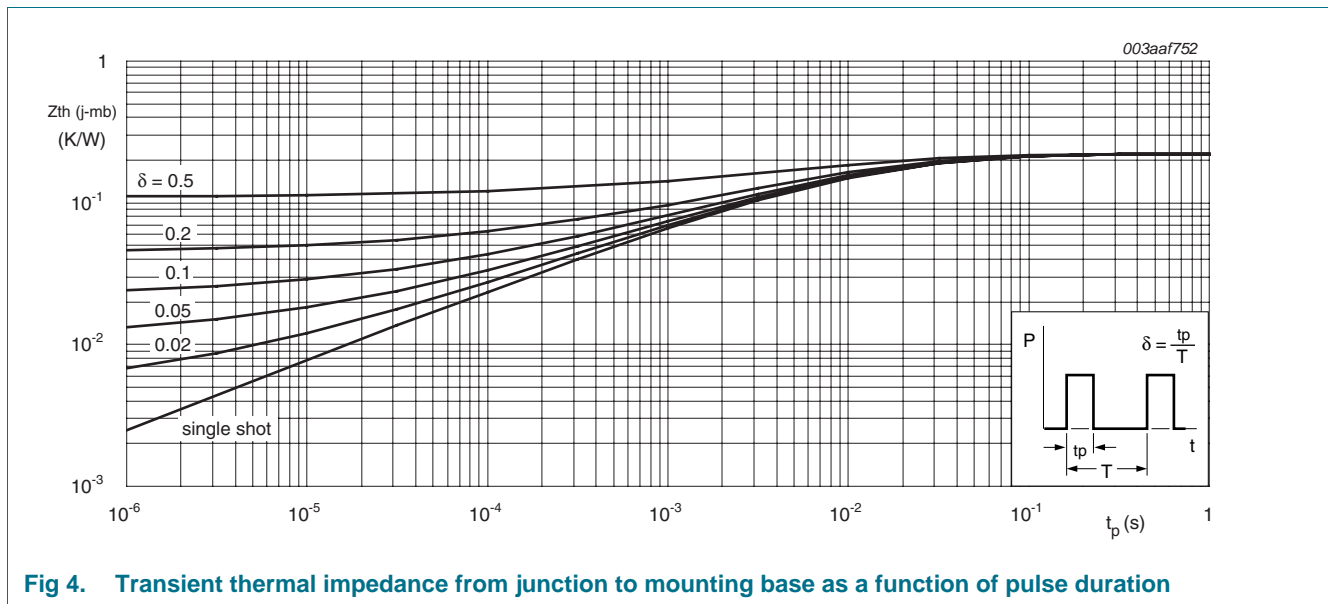


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

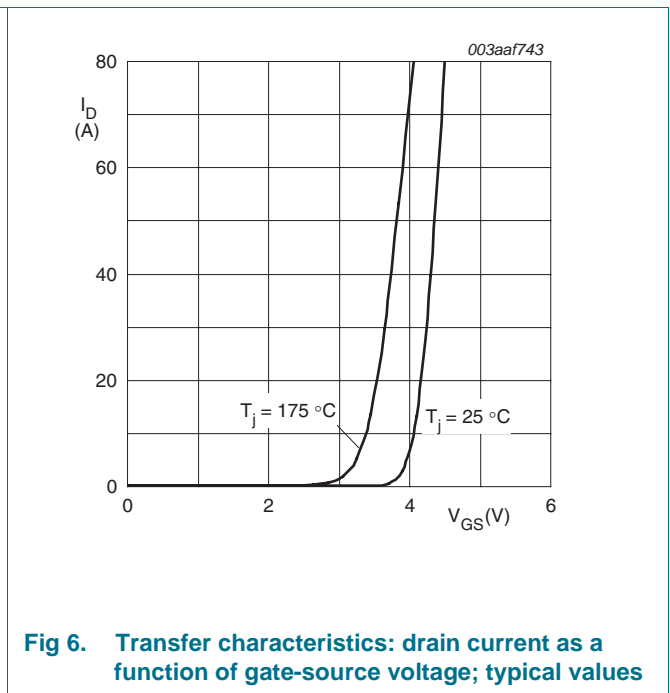
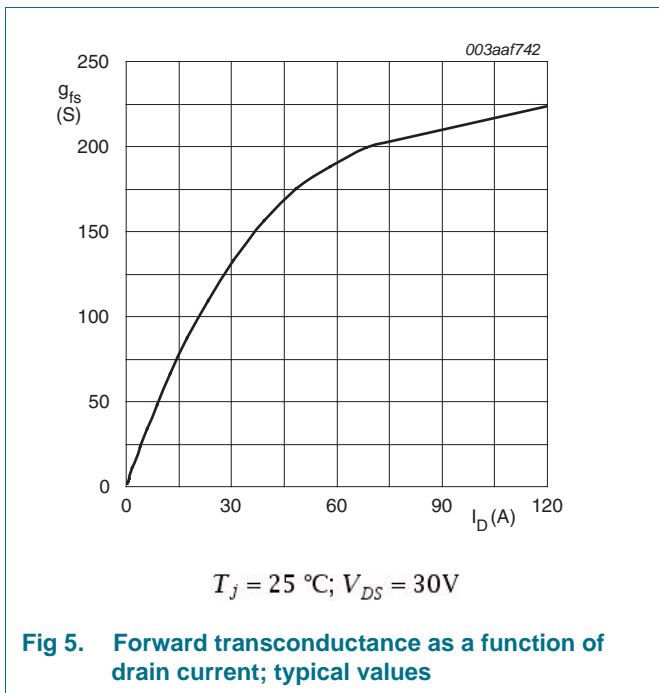
Table 6. Characteristics

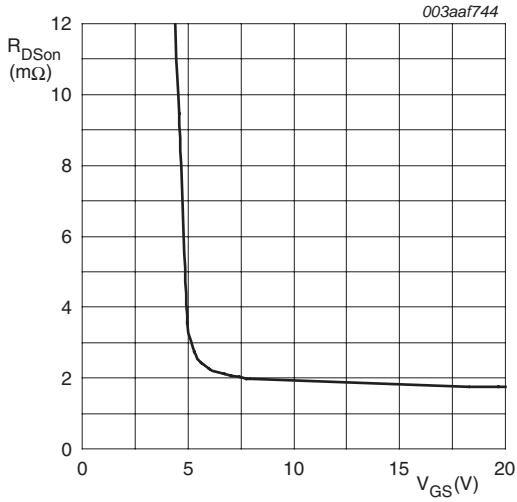
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|-----------------------------------|---|------------------|------|-----|---------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$ | 54 | - | - | V |
| | | $I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | 60 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 10 | - | - | 4.6 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 10 | 1 | - | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 11 ; see Figure 10 | 2 | 3 | 4 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 0.03 | 10 | μA |
| | | $V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$ | - | - | 500 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | - | 100 | nA |
| | | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | - | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 12 | ^[1] - | 1.8 | 2.2 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 12 ; see Figure 13 | - | 4.3 | 5.1 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see Figure 12 ; see Figure 13 | - | 3 | 3.5 | mΩ |
| R_G | gate resistance | $f = 1 \text{ MHz}$ | - | 0.9 | - | Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 75 \text{ A}; V_{DS} = 30 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15 | - | 137 | - | nC |
| | | $I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15 | - | 129 | - | nC |
| Q_{GS} | gate-source charge | $I_D = 75 \text{ A}; V_{DS} = 30 \text{ V}; V_{GS} = 10 \text{ V}$ | - | 48 | - | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | $I_D = 75 \text{ A}; V_{DS} = 30 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15 | - | 29 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | - | 19 | - | nC |
| Q_{GD} | gate-drain charge | | - | 32 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $V_{DS} = 30 \text{ V};$ see Figure 14 ; see Figure 15 | - | 5.7 | - | V |
| C_{iss} | input capacitance | $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 16 | - | 9997 | - | pF |
| C_{oss} | output capacitance | | - | 1210 | - | pF |
| C_{rss} | reverse transfer capacitance | | - | 594 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 30 \text{ V}; R_L = 0.4 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 4.7 \text{ } \Omega; I_D = 75 \text{ A}$ | - | 42 | - | ns |
| t_r | rise time | | - | 56 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 115 | - | ns |
| t_f | fall time | | - | 49 | - | ns |

Table 6. Characteristics ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|-----------------------|---|-----|-----|-----|------|
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17 | - | 0.8 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 30\text{ V}$ | - | 57 | - | ns |
| Q_r | recovered charge | $I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 30\text{ V}$ | - | 80 | - | nC |

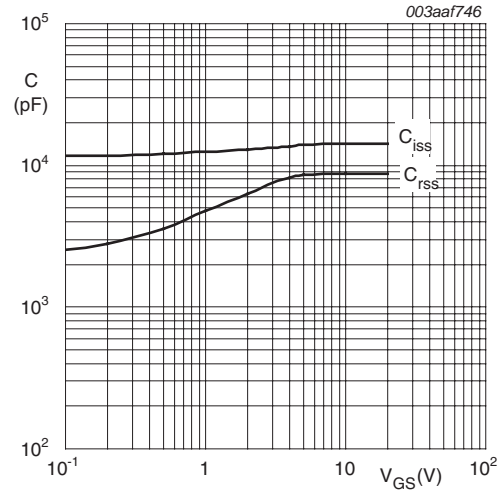
[1] Measured 3 mm from package.





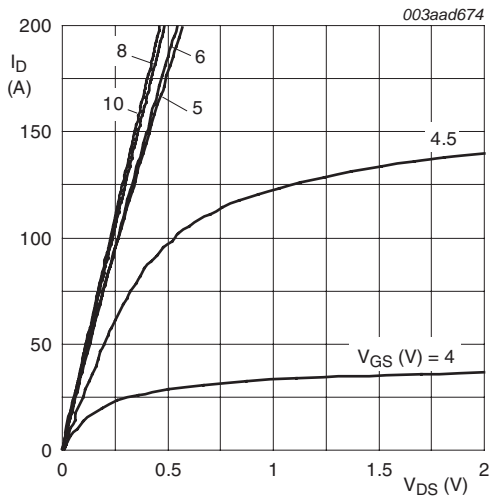
$T_j = 25\text{ °C}; I_D = 25\text{ A}$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



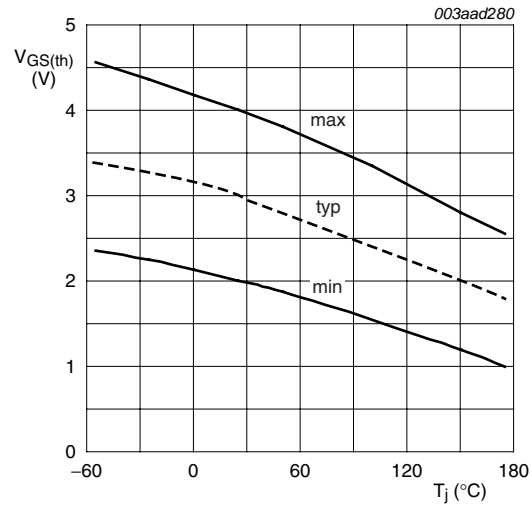
$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage, typical values



$T_j = 25\text{ °C}; t_p = 300\text{ }\mu\text{s}$

Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values



$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature

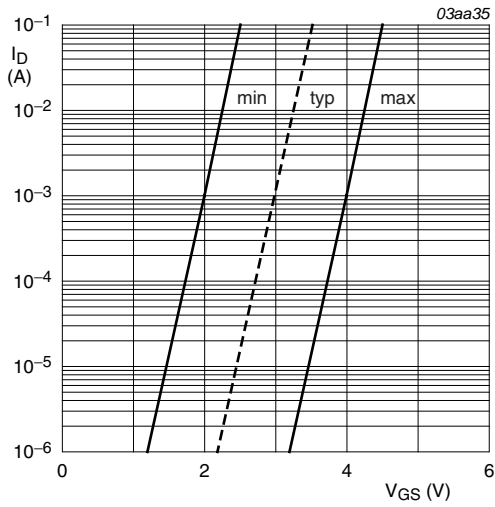


Fig 11. Sub-threshold drain current as a function of gate-source voltage

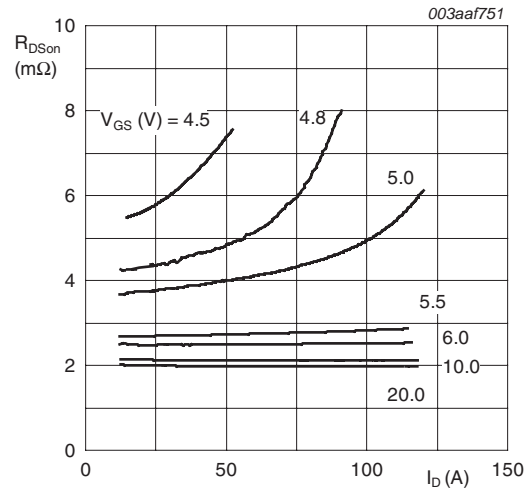


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

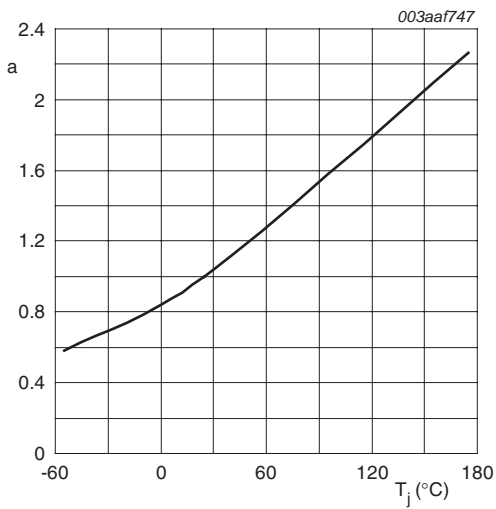


Fig 13. Drain-source on-state resistance as a function of gate-source voltage; typical values

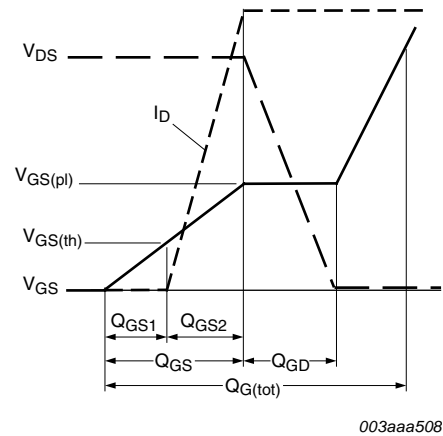
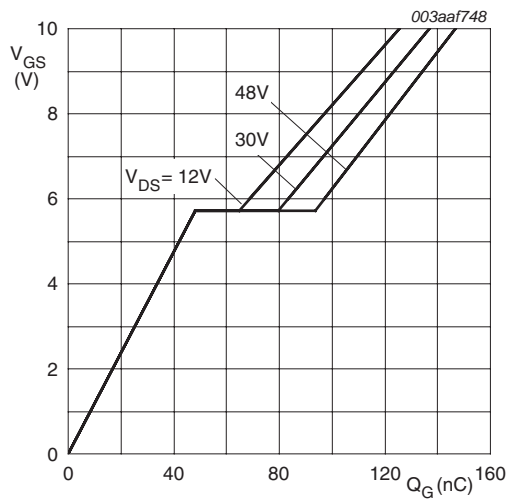
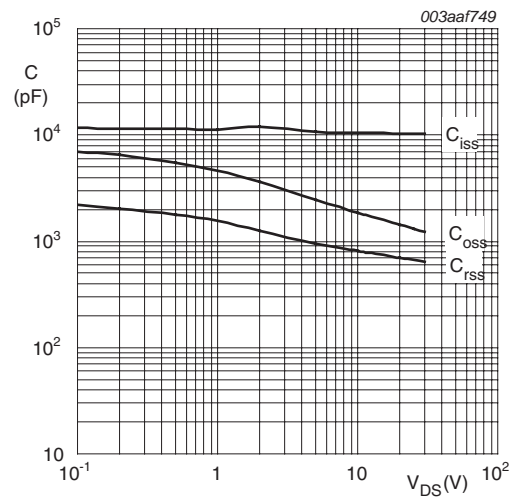


Fig 14. Gate charge waveform definitions



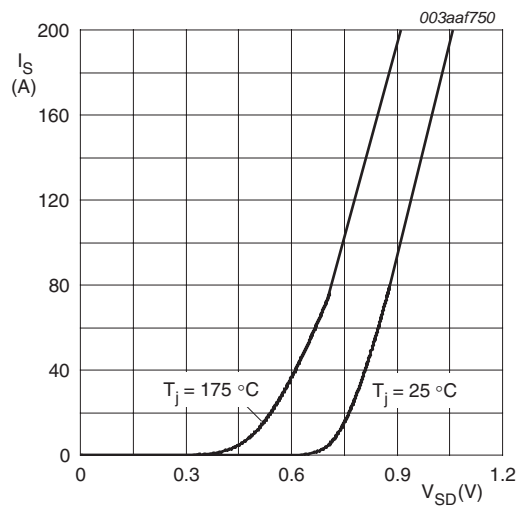
$T_j = 25\text{ }^\circ\text{C}; I_D = 75\text{ A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended package (I2PAK); low-profile 3-lead TO-262

SOT226

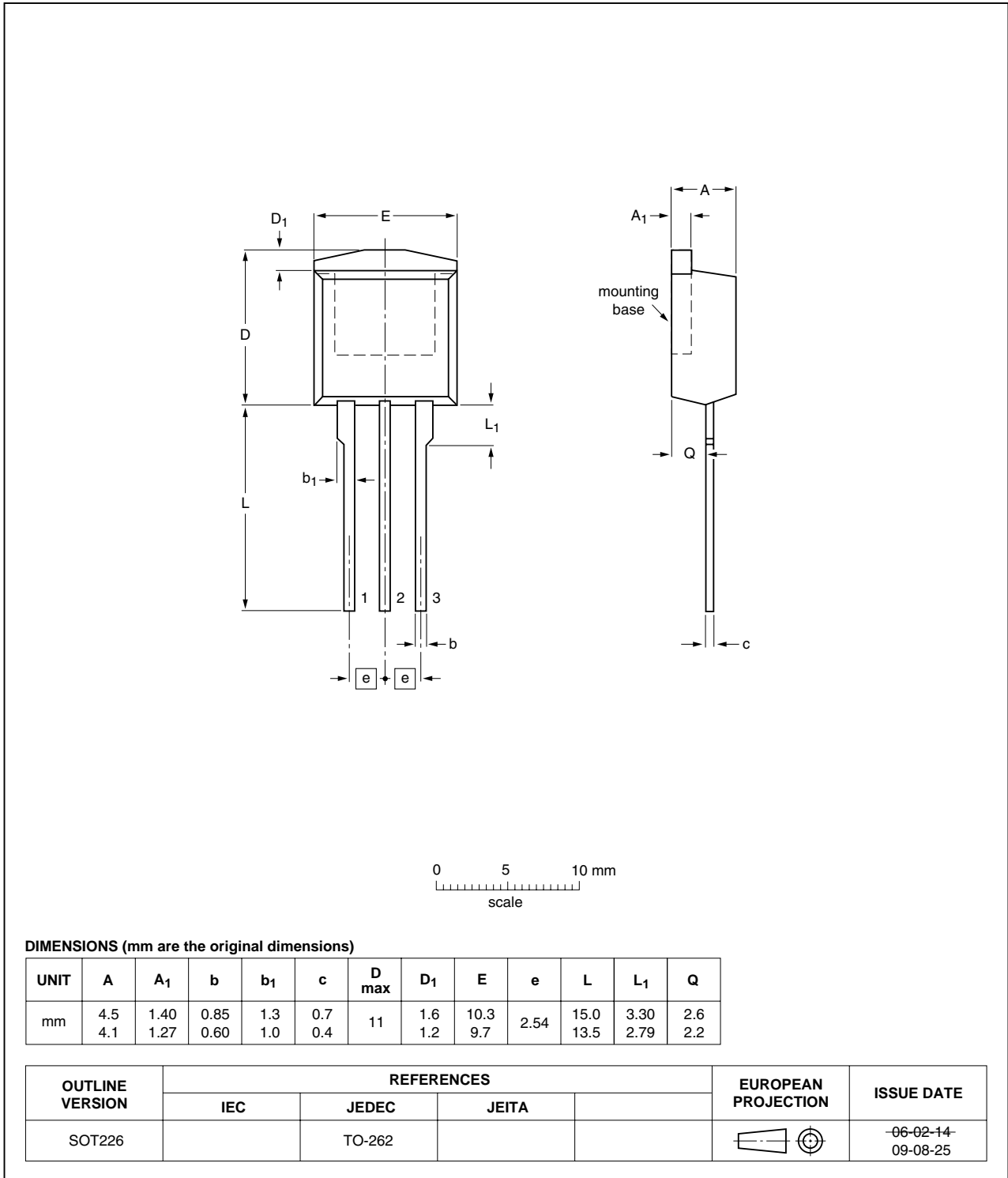


Fig 18. Package outline SOT226 (I2PAK)

8. Revision history

Table 7. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|---|----------------------|---------------|------------------|
| PSMN2R0-60ES v.2 | 20110419 | Product data sheet | - | PSMN2R0-60ES v.1 |
| Modifications: | <ul style="list-style-type: none">• Status changed from objective to product.• Various changes to content. | | | |
| PSMN2R0-60ES v.1 | 20110117 | Objective data sheet | - | - |

9. Legal information

9.1 Data sheet status

| Document status ^[1] ^[2] | Product status ^[3] | Definition |
|---|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

| | | |
|-----------|--|-----------|
| 1 | Product profile | 1 |
| 1.1 | General description | 1 |
| 1.2 | Features and benefits | 1 |
| 1.3 | Applications | 1 |
| 1.4 | Quick reference data | 1 |
| 2 | Pinning information | 2 |
| 3 | Ordering information | 2 |
| 4 | Limiting values | 3 |
| 5 | Thermal characteristics | 5 |
| 6 | Characteristics | 6 |
| 7 | Package outline | 11 |
| 8 | Revision history | 12 |
| 9 | Legal information | 13 |
| 9.1 | Data sheet status | 13 |
| 9.2 | Definitions | 13 |
| 9.3 | Disclaimers | 13 |
| 9.4 | Trademarks | 14 |
| 10 | Contact information | 14 |

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